REMARKS

Claims 1-18, 23, and 42-47, remain pending in this application. Additionally, new claims 56-61 have been added. Therefore, claims 1-18, 23, 42-47, and 56-61 are pending in the present application.

Claims 17, 23, and 42 have been amended to correct a punctuation error. Applicants acknowledge and appreciate the Examiner's withdrawal of the restriction requirement of claim 23 and the allowance of claim 23.

The Examiner objected to claims 11-13 and 44 because the claims recite the limitation "said acquired model." Claims 11 and 44 have been amended to provide sufficient antecedent basis for the limitation in the claim. Therefore, claims 11-13 and 44 are now in condition for allowance. Claims 11-13 and 44 are allowable for at least the reasons cited above.

The Examiner rejected claims 1-3, 7, 9, 10, 14, 15, 18, 42, 43, and 45-47 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,581,029 (***Fischer***). Applicants respectfully traverse this rejection.

In the Final Office Action dated October 20, 2003, the Examiner argued that since the purpose of simulating is to optimize variables for manufacturing, as disclosed in ***Fischer***, it would have been inherent to interface the simulation with the process control environment. Applicants respectfully disagree. Merely because ***Fischer*** discloses simulating to optimize various variables does not follow that the simulation function is actually interfaced with the process control environment as called for by the amended claim 1 of the present invention.

Optimizing variables may include calculating new values for the variable based upon simulation. However, ***Fischer*** still does not disclose or suggest interfacing the simulation function with the process control environment. Furthermore, ***Fischer*** does not disclose generating a first model to perform a simulation and then generating a second model for processing semiconductor devices, wherein the operation of the first model is actually capable of affecting the second model; and then interfacing the simulation function with the process control environment using the first or the second model. These elements called for by claim 1, as amended, are not disclosed or suggested by ***Fischer***.

The Examiner cites ***Fischer*** to disclose a simulation process for the creation of a simulated device. Variables in the associated process steps may be varied to generate a simulated semiconductor device. See column 1, lines 27-54. ***Fischer*** generally relates to modules that are used to perform simulation, as well as to a system for eliminating redundant modules in a simulation system. See column 5, lines 10-39. However, ***Fischer*** does not disclose performing process simulations to produce simulation data using the first and second models, and interfacing the simulation data with an actual process control environment for controlling the manufacturing process of an actual semiconductor device, as called for by claims 1 and 42 (as amended) of the present invention.

Fischer merely discloses performing simulations to generate a simulated semiconductor device. See column 1, lines 33-36. ***Fischer*** discloses utilizing executable modules that may represent steps in process simulation flow and optimizing the modules to reduce redundancy of the modules. ***Fischer*** does not disclose interfacing the simulation data to actual manufacturing of semiconductor devices. The disclosure of ***Fischer*** is in the realm of the creation of a

simulated device. Therefore, ***Fischer*** does not disclose the process simulation function and the interfacing of simulation data resulting from a process simulation function with an actual process control environment for controlling the actual manufacturing process of a semiconductor device. Therefore, ***Fischer*** does not disclose all of the elements of claim 1. One of ordinary skill in the art would not be able to disclose all of the elements of performing a process simulation to produce simulation data and interfacing the simulation data with a process control for actual manufacturing process control of the actual processing of the semiconductor device based upon the redundancy module optimization disclosed by ***Fischer***. Therefore, claim 1 of the present application is allowable. Additionally, claim 42, which also calls for applying simulation results and interfacing the results with an actual process control environment, is also allowable for at least the reasons cited above. Furthermore, newly added claims 56-61, which comprise subject matter that the Examiner said is allowable (*e.g.*, subject matter similar to claims 11-13, 16, and 17), are also allowable for at least the reasons cited above.

Independent claims 1 and 42 (both as amended) are allowable for at least the reasons cited above. Claims 2-18, which depend from independent claim 1, and claims 43-47, which depend from independent claim 42, are also allowable for at least the reasons cited above. Additionally claims 56-61 are also allowable for at least the reasons cited above.

Applicants also assert that the newly added claims 56-61 are also allowable for at least the reasons cited above. In fact, the newly added claims 56-61 have similarities with the claims that were objected to by the Examiner, which the Examiner stated would be allowable if they had been written in an independent fashion (claims 11-13, 16, and 17). Therefore, Applicants respectfully assert that claims 56-61 are also allowable.

The Examiner rejected claims 4-6 and 8, under 35 U.S.C. § 103(a) as being unpatentable over ***Fischer***. Applicants respectfully traverse this rejection.

Applicants respectfully assert that claims 4-6 and 8 are not obvious to one skilled in the art upon a reading of ***Fischer***. The Examiner states that ***Fischer*** does not explicitly teach the process task of defining photolithography, etch, chemical mechanical polishing (CMP), and diffusion process tasks and states that it would have been obvious to one of ordinary skill in the art to include these process tasks upon a reading of ***Fischer***. Applicants respectfully disagree. Since ***Fischer*** does not disclose all of the elements of the underlying claims, which were amended, from which claims 4-6, and 8 depend (*i.e.*, claim 1), using the argument that one of ordinary skill in the art would implement photolithography, etch, CMP, and diffusion process tasks, to the teaching of ***Fischer*** would still not result in all of the elements called for by claims 4-6 and 8. As described above, the underlying claim 1, from which claims 4-6, and 8 are dependent, are not disclosed, taught, or suggested by ***Fischer***, therefore, merely adding the concepts of photolithography, etch, CMP, and diffusion processes, would not be able to make obvious the subject matter called for by claims 4-6, and 8. Therefore, claims 4-6, and 8 are allowable for at least the reasons cited above.

Applicants acknowledge that the Examiner allowed claim 23. In light of the arguments presented above, Applicants respectfully assert that claims 1-18, 42-47, and 56-61 are also allowable. In light of the arguments presented above, a Notice of Allowance is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Houston, Texas telephone number (713) 934-4069 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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IN THE CLAIMS

1. (Currently Amended) A method, comprising:

defining a process task;

performing a process simulation function to produce simulation data corresponding to said process task, performing said process simulation function comprising:

generating a first model to perform a simulation;

generating a second model for processing a semiconductor device, an operation of said first model first model being capable of affecting said second model; and

interfacing said simulation data with a process control environment for controlling a manufacturing process of said semiconductor device using at least one of said first and second model.

2. (Original) The method described in claim 1, further comprising performing a manufacturing process of the semiconductor device based upon said interfacing of said simulation data with said process control environment.

3. (Original) The method described in claim 2, wherein performing manufacturing process of said semiconductor device further comprises processing a semiconductor wafer.

4. (Original) The method described in claim 3, wherein defining a process task further comprises defining a photolithography process task.

5. (Original) The method described in claim 3, wherein defining a process task further comprises defining an etch process task.

6. (Original) The method described in claim 3, wherein defining a process task further comprises defining a chemical-mechanical polishing process task.

7. (Original) The method described in claim 3, wherein defining a process task further comprises defining an implant process task.

8. (Original) The method described in claim 3, wherein defining a process task further comprises defining a diffusion process task.

9. (Original) The method described in claim 3, wherein performing a process simulation function further comprises:

preparing at least one processing model for simulation;

executing a simulation using said processing model to generate a simulation result;

determining whether said simulation result is within a predetermined specification; and

applying said simulation result into at least one manufacturing parameter in response to a determination that said simulation result is within said predetermined specification.

10. (Original) The method described in claim 9, further comprising modifying said model in response to a determination that said simulation result is not within said predetermined specification.

11. (Currently amended) The method described in claim 9, wherein preparing at least one processing model for simulation further comprises:

defining at least one processing model to generate a defined model;

validating said defined model;

acquiring data for operation of said defined model;

preparing an acquired model from said data; and

populating said defined model with at least a portion of said acquired model.

12. (Original) The method described in claim 11, wherein defining at least one processing model further comprises defining at least one of a device physics model, a process model, and an equipment model.

13. (Original) The method described in claim 11, wherein validating said defined model further comprises integrating a plurality of defined models into a simulation environment.

14. (Previously presented) The method described in claim 9, wherein executing said simulation using said processing model to generate a simulation result further comprises:

modulating at least one variable in said processing model;

executing a model behavior based upon said variable;

determining at least one component of variation based upon said execution of the model behavior; and

determining whether said at least one component of variation is within a predetermined specification.

15. (Original) The method described in claim 14, wherein modulating at least one variability in said processing model further comprises modulating a temperature component.

16. (Original) The method described in claim 14, further comprising performing a predictive state analysis in response to said execution of said model behavior.

17. (Currently amended) The method described in claim 14, further comprising performing a sensitivity analysis in response to said execution of said model behavior.

18. (Original) The method described in claim 9, wherein applying said simulation result into at least one manufacturing parameter further comprises modifying at least one manufacturing control parameter based upon said simulation result.

19. (Withdrawn) A system, comprising:

a computer system;

a manufacturing model coupled with said computer system, said manufacturing model being capable of generating and modifying at least one control input parameter signal;

a machine interface coupled with said manufacturing model, said machine interface being capable of receiving process recipes from said manufacturing model;

a processing tool capable of processing semiconductor wafers and coupled with said machine interface, said first processing tool being capable of receiving at least one control input parameter signal from said machine interface;

a metrology tool coupled with said first processing tool and said second processing tool, said metrology tool being capable of acquiring metrology data;

a metrology data analysis unit coupled with said metrology, said metrology data analysis unit being capable of organizing said acquired metrology data; and

a simulation environment coupled to said metrology data analysis unit and said computer system, said simulation environment capable of producing simulation data for controlling manufacturing of semiconductor wafers.

20. (Withdrawn) The system of claim 19, wherein said computer system is capable of generating modification data for modifying at least one control input parameter in response to a said simulation data.

21. (Withdrawn) The system of claim 20, wherein said manufacturing model is capable of modifying said control input parameter in response to said modification data.

22. (Withdrawn) The system of claim 19, wherein said simulation environment comprises:

a simulator, said simulator being capable of simulating a manufacturing process of a semiconductor wafer:

a device physics model coupled to said simulator, said device physics model being capable of emulating semiconductor wafer manufacturing characteristics;

a process model coupled to said simulator, said process model being capable of emulating a semiconductor wafer manufacturing process;

an equipment model coupled to said simulator, said equipment model being capable of emulating a semiconductor wafer manufacturing process tool; and

a process control interface coupled to said simulator, said process control interface being capable of facilitating communication between said simulation environment and a process control environment.

23. (Currently amended) An apparatus, comprising:

means for defining a process task;

means for performing a process simulation function to produce simulation data corresponding to said process task; and

means for interfacing said simulation data with a process control environment for controlling a manufacturing process of a semiconductor device[[;]].

24. (Withdrawn) A computer readable program storage device encoded with instructions that, when executed by a computer, performs a method, comprising:

defining a process task;

performing a process simulation function to produce simulation data corresponding to said process task; and

interfacing said simulation data with a process control environment for controlling a manufacturing process of a semiconductor device;

25. (Withdrawn) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 24, further comprising performing a manufacturing process of the semiconductor device based upon said interfacing of said simulation data with said process control environment.

26. (Withdrawn) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 25, wherein performing manufacturing process of said semiconductor device further comprises processing a semiconductor wafer.

27. (Withdrawn) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 26, wherein defining a process task comprises defining a photolithography process task.

28. (Withdrawn) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 26, wherein defining a process task comprises defining an etch process task.

29. (Withdrawn) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 26, wherein defining a process task comprises defining a chemical-mechanical polishing process task.

30. (Withdrawn) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 26, wherein defining a process task further comprises defining an implant process task.

31. (Withdrawn) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 26, wherein defining a process task further comprises defining a diffusion polishing process task.

32. (Withdrawn) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 26, wherein performing a process simulation function further comprises:

preparing at least one processing model for simulation;

executing a simulation using said processing model to generate a simulation result;

determining whether said simulation result is within a predetermined specification; and

applying said simulation result into at least one manufacturing parameter in response to a determination that said simulation result is within said predetermined specification.

33. (Withdrawn) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 32, further comprising modifying said model in response to a determination that said simulation result is not within said predetermined specification.

34. (Withdrawn) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 32, wherein preparing at least one processing model for simulation further comprises:

defining at least one processing model;

validating said defined model;

acquiring data for operation of said defined model; and

populating said defined model with said acquired model.

35. (Withdrawn) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 34, wherein defining at least one processing model comprises defining at least one of a device physics model, a process model, and an equipment model.

36. (Withdrawn) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 34, wherein validating said defined model further comprises integrating a plurality of defined models into a simulation environment.

37. (Withdrawn) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 32, wherein executing said simulation using said processing model to generate a simulation result further comprises:

modulating at least one variability in said processing model;

executing a model behavior based upon said variability;

determining at least one component of variation based upon said execution of the model behavior; and

determining whether component of variation is within a predetermined specification.

38. (Withdrawn) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 37, wherein modulating at least one variability in said processing model further comprises modulating a temperature component.

39. (Withdrawn) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 37,

further comprising performing a predictive state analysis in response to said execution of said model behavior.

40. (Withdrawn) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 37, further comprising performing a sensitivity analysis in response to said execution of said model behavior

41. (Withdrawn) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 32, wherein applying said simulation result into at least one manufacturing parameter further comprises modifying at least one manufacturing control parameter based upon said simulation result.

42. (Currently amended) A method, comprising:

defining a process task;

performing a process simulation function to produce simulation data corresponding to said process task, said process simulation function comprising:

preparing at least one processing model for simulation;

executing a simulation using said processing model to generate a simulation result;

<u>generating a defined model based upon said simulation;</u>

determining whether said simulation result is within a predetermined specification; and

applying said simulation result into at least one manufacturing parameter in response to a determination that said simulation result is within said predetermined specification; [[and]]

preparing an acquired model from said data;

populating said defined model with said acquired model; and

interfacing said simulation data with a process control environment for controlling a manufacturing process of a semiconductor device using said defined model[[;]].

43. (Previously presented) The method described in claim 42, further comprising modifying said model in response to a determination that said simulation result is not within said predetermined specification.

44. (Currently amended) The method described in claim 42, wherein preparing at least one processing model for simulation further comprises:

defining at least one processing model, to generate a defined model;

validating said defined model;

acquiring data for operation of said defined model;

preparing an acquired model from said data; and

populating said defined model with said acquired model.

45. (Previously presented) The method described in claim 44, wherein defining at least one processing model further comprises defining at least one of a device physics model, a process model, and an equipment model.

46. (Previously presented) The method described in claim 44, wherein validating said defined model further comprises integrating a plurality of defined models into a simulation environment.

47. (Previously presented) The method described in claim 42, wherein executing said simulation using said processing model to generate a simulation result further comprises:

modulating at least one variable in said processing model;

executing a model behavior based upon said variable;

determining at least one component of variation based upon said execution of the model behavior; and

determining whether said at least one component of variation is within a predetermined specification.

48. (Withdrawn) A method, comprising:

defining a graph relating to a desired results of a processed semiconductor wafer;

defining a graph relating to a predicted results of said processed semiconductor wafer;

comparing said graph relating to said desired results to said graph relating to said predicted results to determine a difference between said graphs; and

adjusting at least one control input parameter for a manufacturing process based upon said difference between said graphs.

49. (Withdrawn) The method described in claim 48, wherein defining said graph relating to the desired results of said processed semiconductor wafer further comprises defining said graph relating to at least one electrical parameter of a semiconductor wafer.

50. (Withdrawn) The method described in claim 49, wherein defining said graph relating to at least one electrical parameter of a semiconductor wafer further comprises defining said graph relating to a speed of operation of a circuit formed on said semiconductor wafer.

51. (Withdrawn) The method described in claim 48, wherein defining said graph relating to the predicted results of said processed semiconductor wafer further comprises defining said graph relating to at least one electrical parameter of a semiconductor wafer.

52. (Withdrawn) The method described in claim 51, wherein defining said graph relating to at least one electrical parameter of a semiconductor wafer further comprises defining said graph relating to a speed of operation of a circuit formed on said semiconductor wafer.

53. (Withdrawn) The method described in claim 48, further comprising:

defining a graph relating to an actual result of said processed semiconductor wafer;

comparing said graph relating to said actual result to said graph relating to said desired results and to said graph relating to said predicted results;

adjusting at least one control input parameter for a manufacturing process based upon said comparison.

54. (Withdrawn) The method described in claim 53, wherein defining said graph relating to the actual results of said processed semiconductor wafer further comprises defining said graph relating to at least one electrical parameter of a semiconductor wafer.

55. (Withdrawn) The method described in claim 55, wherein defining said graph relating to at least one electrical parameter of a semiconductor wafer further comprises defining said graph relating to a speed of operation of a circuit formed on said semiconductor wafer.

56. (New) A method, comprising:

defining a process task;

performing a process simulation function to produce simulation data corresponding to said process task, performing said process simulation function comprising:

preparing at least one processing model for simulation to generate a defined model;

validating said defined model by determining whether said simulation result is within a predetermined specification;

acquiring data for operation of said defined model;

preparing an acquired model from said data for operation;

population said defined model with at least a portion of said acquired model; and

interfacing said simulation data with a process control environment for controlling a manufacturing process of said semiconductor device using at least one of said defined model and said acquired model.

57. (New) The method described in claim 56, wherein defining at least one processing model further comprises defining at least one of a device physics model, a process model, and an equipment model.

58. (New) The method described in claim 56, wherein validating said defined model further comprises integrating a plurality of defined models into a simulation environment.

59. (New) The method described in claim 56, wherein executing said simulation using said processing model to generate a simulation result further comprises:

modulating at least one variable in said processing model;

executing a model behavior based upon said variable;

determining at least one component of variation based upon said execution of the model behavior; and

determining whether said at least one component of variation is within a predetermined specification.

60. (New) The method described in claim 59, further comprising performing a predictive state analysis in response to said execution of said model behavior.

61. (New) The method described in claim 59, further comprising performing a sensitivity analysis in response to said execution of said model behavior.